ABSTRACT OF THE DISCLOSURE

The present invention provides a method and apparatus for amortizing critical path computation. According to an embodiment of the present invention, a digital circuit design is simulated using cycle based simulation techniques. The digital circuit design is represented by a data flow graph. In the data flow graph are one or more critical paths and one or more shortest paths. The data flow graph representing the digital circuit design is unrolled into a plurality of simulation cycles. Thereafter, the multiple cycle graph is scheduled to a plurality of processing units, thereby simulating several cycles at once. In one embodiment, communication latency is relaxed by delaying the arrival times of external inputs within the unrolled cycles. In another embodiment, the unrolled circuit allows for scheduling compaction. The present invention provides for improved simulation speed by better balancing the workload among multiple processing units in the system.